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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,094	11/25/2003	Yasunori Bito	Q78644	4905

7590 12/22/2004

SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 Pennsylvania Avenue, N.W.
Washington, DC 20037

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,094	BITO, YASUNORI	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *19-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14 and 15* is/are rejected.

7)☒ Claim(s) *13 and 16-18* is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group II, claims 1-18 in the Paper received 10-13/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a).

Oath/Declaration

2. The oath/declaration filed on 11/25/2003 is acceptable.

Drawings

3. The formal drawings filed on 11/25/2003 are acceptable.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. The Information Disclosure Statement filed on 11/25/2003 has been considered.

Claim Objections

6. Claim 1 is objected to because of the following informalities: By its literal terms claim 1 requires first and second cap layers formed with the second cap layer on the first cap layer (line 10), a second electrode on the second cap (lines 12-13), and a first electrode on the first cap (and literally, under the second cap layer). Applicant's drawings and spec reflect intent on applicant's part to claim both the first and second electrode formed on different portions of the second cap layer. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1,2,4, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by BITO ET AL. (2001/005,016).

Bito et al. discloses a heterojunction field effect type semiconductor device comprising a GaAs substrate 101; an undoped InGaAs channel layer 105 formed over said GaAs substrate 101; an undoped GaAs first semiconductor layer 109 including no aluminum formed over said channel layer 105; first 110 and second 111 cap layers of a

first conductivity type formed on said first semiconductor layer 109, said first 110 and second 111 cap layers creating a first recess (no part #, it is the recess filled by the gate electrode 114 and the second semiconductor layer 121) on said first semiconductor layer 109; first 113 and second 114 ohmic electrodes formed on said first 110 and second 111 cap layers; a GaAs second semiconductor layer 121 of second conductivity type formed on said first semiconductor layer 109 within said first recess, said second semiconductor layer 121 being isolated from said first 110 and second 111 cap layers; and a gate electrode 114 formed on said second semiconductor layer 121. Note figure 6 and paragraphs 0073-0079 of Bito et al.

9. Claims 1,3,5,6-9,11,12,14, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by KATO ET AL. (2001/019,131).

Kato et al. discloses a heterojunction field effect type semiconductor device comprising a GaAs substrate 501; a first conductivity (n) type GaAs channel layer 506 formed over said GaAs substrate 501; a first semiconductor layer 509 including no aluminum formed over said channel layer 506; first 511 and second 512 GaAs cap layers of the first conductivity (n) type formed on said first semiconductor layer 509, said first 511 and second 512 cap layers creating a first recess on said first semiconductor layer 509; first 572 and second 573 ohmic electrodes formed on said first 511 and second 512 cap layers; a second AlGaAs or InGaP (note paragraph 0027 discloses both alternatives) semiconductor layer 520 of second conductivity (p) type formed on said first semiconductor layer 509 within said first recess, said second semiconductor

layer 520 being isolated from said first 511 and second 512 cap layers; and a gate electrode 571 formed on said second semiconductor layer 520.

With further regard to claims 6-9, Kato et al.'s heterojunction field effect type semiconductor device further comprises an AlGaAs or InGaP wide recess etching stopper layer 510 (AlGaAs layer) or 530 (InGaP layer) of said first conductivity (n) type beneath said first 511 and second 512 cap layers, said InGaP layer 530 being in contact with said second semiconductor layer 520.

With further regard to claims 14-15, Kato et al.'s heterojunction field effect type semiconductor device further comprises a third semiconductor layer 510 having a thickness (30 nm) of more than 5 nm and interposed between said first semiconductor layer 509 and said first 511 and second 512 cap layers and having a second recess, said second semiconductor layer 520 passing through the second recess of said third semiconductor layer 510 to reach said first semiconductor layer 509.

Note figures 30-34 and paragraphs 0027 and 201-205 of Kato et al.

Allowable Subject Matter

10. Claims 13 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
12/04